On-board DSP Technologies applied to Robotics Applications
A review of existing building blocks

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ABSTRACT

To fulfil the growing needs of processing high quantities of data on-board satellites, ESA has designed and is now developing a set of data acquisition and processing elements for on-board applications. These, though initially on-board-satellite data processing oriented, could be suitable building blocks for the design of Automation & Robotics systems. This paper provides an overview on related developments within the Agency, including hardware aspects: advanced cameras, integrated Digital Processing Units (DPU), high-speed serial communication devices; and software aspects: Real Time Operating System, image-processing software library, and especially vision modules.

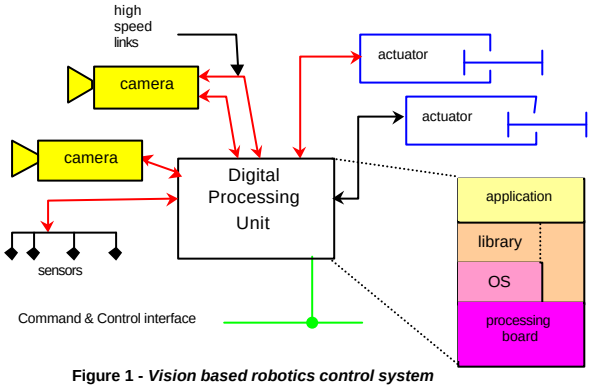


Figure 1 - *Vision based robotics control system*

AKNOWLEDGMENTS

Building blocks presented in this paper are the result of a collaborative effort within the Agency and in particular TOS-ESM (S. Habinc), TOS-ESD (P. Plancke) and TOS-ETD (W. Gasti, J. Rosello Guasch, P. Armbruster) sections and our industrial partners. This is illustrated by the versatility of disciplines involved in their realisation.

INTRODUCTION

The development of digital signal processing has led to the general trend, in vision based systems, which is to perform digitalisation as close as possible to the sensor in order to have imagers with digital output. The digitalisation of the whole processing chain (sensors, data links, image/signal processor, actuators) can then be designed according to very specific needs – e.g. dedicated video transport/processing for robotics – or in the perspective of a modular and flexible system. Of course, dedicated solutions will always achieve more performance, but the cost will be high and the re-usability low, from one project to another. So, ESA has initiated an ambitious programme for the design and development of a number of ready-to-use components that are flexible enough to be assembled in versatile systems and thus fulfil a wide range of processing needs. This paper presents some of these components that are expected to be suitable for implementation in a robotic systems (Figure 1).

Versatile cameras

ESA has sponsored the development of single-chip APS-based image sensors, emphasising the following aspects: low power, mass, volume and cost, versatility in interfacing to on-board data handling and communication systems, radiation tolerance. These cameras may be small and very cheap, such as the space tolerant **VMC** family (Figure 2) designed by OIP N.V.[1], Alcatel Microelectronics and FillFactory[2]/IMEC[3], or very miniaturised such as the matchbox size camera (Figure 4) designed by CSEM [4].

The Visual Monitoring Camera family

Figure 2 - *VMC IRIS 2 camera*

The cameras of the VMC family have all the same mechanical packaging (see technical characteristics below) although their pixel-resolution, colour-resolution and light-sensitivity can differ. They contain a frame buffer that can hold one complete image.
FUGA15 sensors (512x512) are Black&White and "autonomous". They have a logarithmic light-sensitivity, which enable them to acquire a useful image whatever the lighting conditions are (very dark, very bright, or very contrasted) without parameter settings.
IRIS-1 sensors (640x480) can be mounted with a colour filter and are more sensitive: exposure time can be set from 0.4 ms to 95.8 s, which enables to produce highly-contrasted low-noise images from a specific lighting range.

Technical characteristics:

- IRIS-1 (640 x 480 pixels, 14 micrometer pitch) colour or FUGA15 (512x512) grey scale sensor
- 8 bits digitising on-chip, 10 images per second
- Autonomous or command-interactive operations with image buffering
- TTC-B-01 interface with up to 1 Mbit/s data rate
- Power consumption: 3 W at 28 V

- Dimensions: 6 x 6 x 10 cm
- Weight: 430 g
- 20 Krad (measured on a technology sample)

The use of VMC cameras has already been successfully demonstrated in space:

- VTS (first generation of FUGA VMC), on TeamSat, monitored separation from the launcher (Ariane 502).
- FUGA15 and IRIS-1, on XMM (Ariane 504), visualised the deployed solar panels and the out-gazing of the spacecraft.
- IRIS-1, on Cluster-II, monitored the separation of the spacecraft Rumba and Tango, picturing a beautiful view of the eastern Mediterranean Sea (Figure 3).
- IRIS-1 colour will also fly on MARS Express to monitor the separation of Beagle.

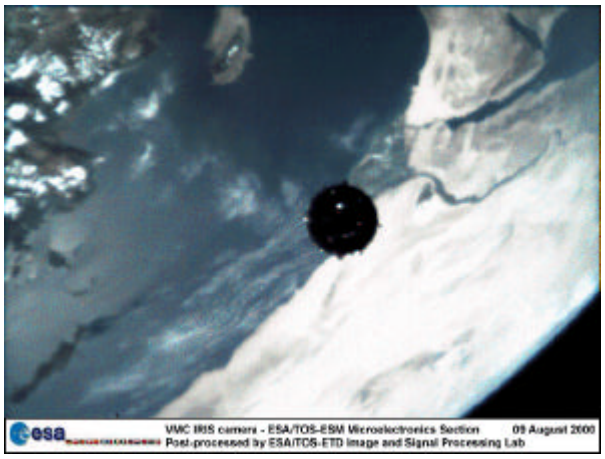


Figure 3 - ***Cluster II separation over the Mediterranean Sea***

Next generation VMC.

At the beginning of 2000, the sensor part of IRIS-1 was merged with the timing and control logic required to operate the sensor and to support multiple variants of interfaces and protocols. The resulting smart imager (named IRIS-2) is essentially a camera-on-a-chip, capable of taking images and directly communicating with the spacecraft. The only electrical parts required to turn an IRIS-2 imager into a camera are line transceivers and passive components. Although IRIS-2 can be used in a multitude of applications, special attention has been given to the aspect of interfacing it with modern spacecraft communication systems. The additional key specifications of IRIS-2 are:

- Sub-windowing, interleaving, digital pixel averaging
- Serial and parallel digital pixel data and command interfaces
- Analogue data output, raw data or CCSDS packets
- Standard spacecraft interfaces
- Redundant logic for fault-tolerance
- Automatic exposure control

The next generation imager (named IRIS-3) will also support off-chip image storage, capable of handling between ten and a hundred images. The imager, together with a dedicated compression device, will support new applications by providing low rate grey scale video capability while maintaining advanced spacecraft interfaces. It will employ a new pixel architecture that preserves the electro-optical sensitivity, while adding to it an increased tolerance towards ionising irradiation, showing only a gradual deterioration over an array of 1024 x 768 pixels at total doses exceeding 20 Mrad. IRIS-3 prototype samples are planned for end 2001.

Micro-miniaturisation

To complement the miniaturisation done with increased integration levels on the sensor silicon itself, an ESA development has been targeted towards the miniaturisation of the mechanical implementation. A matchbox-sized camera has been developed by CSEM [4] (Figure 4). This cost effective solution for resource-critical missions illustrates the possibilities offered by the most recent micro-system technologies, allowing for improvements in mass and power consumption of imaging systems.

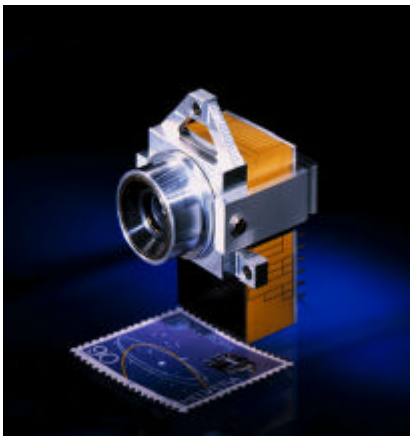


Figure 4 - ***micro-camera from CSEM***

Features:

- 1024 x 1024 full frame CCD
- 10 bit/pixel resolution
- Less than 100 g total weight
- 10 Mbit/s data/strobe RS-422 input and output
- 4 pictures can be stored in the camera
- Storage range : –150 to +50° C
- Operating range: down to -100° C
- Integrated specific CCD voltage supplies

SpaceWire Interface Board for industrial cameras

The SpaceWire Camera Interface Board was designed and developed by Astrium GmbH[6] under the leadership of the University of Dundee[5] in the frame of an ESA contract. The idea is to enable direct real time insertion of camera data at high data rate into an IEEE1355/SpaceWire based processing chain. The board interfaces a high resolution industrial camera (Pulnix TM1300, 1300x1030 pixels, B&W) and formats its data as IEEE 1355 packets using an ASIC device (SMCS*lite*, see section “High speed serial links”). The same IEEE/SpaceWire link is used to transfer camera data and to receive commands, which are forwarded via a serial link interface to the camera.

The main components of the board are

- a 64KBytes FIFO,
- an IEEE 1355/SpaceWire communication device (SMCS*lite*)
- and a controller FPGA.

The design is such that only the FPGA should be reprogrammed when changing to another industrial camera.

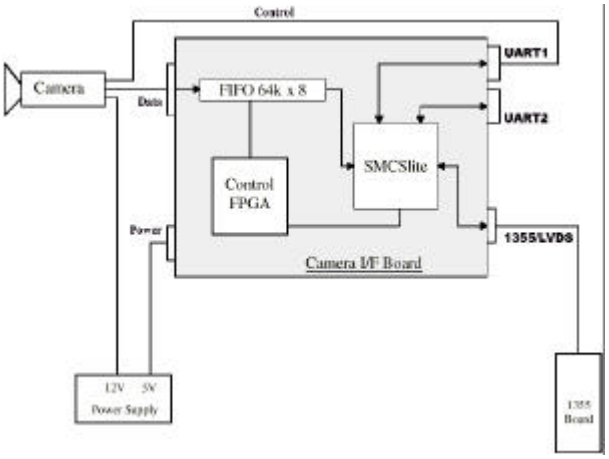


Figure 5 - *SpaceWire Interface Board for Pulnix camera*

This sub-system (camera+interface board), based on COTS elements, is intended to be used in lab demonstrators.

High speed serial links

ESA puts special emphasis on interfaces between processor boards, mass memory boards and sensors, leading to the development of IEEE-1355/SpaceWire high-speed links. **SpaceWire** is an emerging standard for high-speed serial point-to-point bi-directional digital communication that was originally intended to meet needs of future, high-capability, remote sensing and science missions. It is based on two existing commercial standards, IEEE-1355 and LVDS that have been combined and adapted for use on-board spacecraft.

The SpaceWire standard is now finalised and include packet routing (up to network layer of OSI model) and time distribution capabilities. It should be accepted soon as a part of the ECSS-50 standard suite. Efforts are also put to make it become a sub-standard of IEEE 1355.

SMCS332 and SMCS*lite* ASICs were developed (ESA and Astrium GmbH[6]) to ease the implementation of a SpaceWire communication system:

The SMCS332 device was the first IEEE 1355/SpaceWire device developed. It is not fully SpaceWire compatible since it was designed before the standard was finalised but it implements:

- 3 IEEE 1355 links with 200 Mbit/s transfer rate each.
- Link speed configurable for each link separately
- Hardware routing capabilities
- Optional checksum generation and check at packet level
- Configurable (8, 16 or 32 bits) host and data port width
- FIFO or dual ported memory data port
- Interrupt capability for host CPU
- Built-in arbitration for two SMCS332 working on a shared dual ported memory
- JTAG interface and test capability

The SMCS*lite* device was designed for non-intelligent nodes of the network (e.g. a sensor/camera): it can be controlled via the IEEE 1355 link itself. It implements:

- One IEEE 1355 link with 200 Mbit/s transfer rate
- Optional checksum generation and check at packet level
- Control by external host via link using specific SMCS*lite* protocol
- Scalable data interface (8/16 bits)
- Two on-chip timers (independent or cascade)
- Two on-chip UARTs (max bit rate 780 Kbit/s)
- JTAG interface and test capability

Current developments

ESA is now developing with Astrium the SMCS*flex* device, which will be an enhanced version of the SMCS*lite*, fully SpaceWire compatible.
An IP core (synthesisable VHDL) implementing the full SpaceWire standard will be made publicly available soon by ESA. This will enable the integration of the SpaceWire communication layer in any user-specific device and so, promote even more the use of SpaceWire for high-speed data transfer in processing chains, in the space field or in the industry.

Near term developments

To achieve higher data rates in serial link communication, ESA is now studying the feasibility of SpaceWire to operate at more then 400 Mbit/s, in the Gbit/s domain, using if required coaxial cable or optical fibre as physical layer.

processing board(s)

Digital Processing Units

A number of processors and boards have been developed for demanding embedded processing, typically based on the **TSC21020 DSP** (space qualified version of the ADSP21020). Some of these boards were designed specifically for modular, reliable and fault-tolerant parallel signal processing systems, especially for remote sensing applications (Mosaic020 by Astrium[7]). Some of them are designed as mini-modules called Processing Elements, to fulfil stringent requirements on mass, power and volume. Some redundancy can then be achieved by paralleling these mini-modules. Another design directly implements a 2-axis motor control application.

Mosaic020 by Astrium

Astrium GmbH[6] has developed, under ESA contract, the

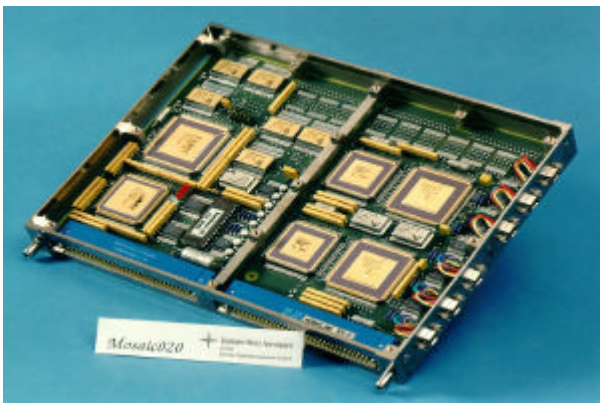


Figure 6 - *Mosaic020 board*

Mosaic020 (Figure 6), a versatile high-performance DSP board specifically designed for modular, reliable and fault-tolerant parallel signal processing systems, especially for aerospace. The specific layout and design of the board allow different configurations, ranging from commercial quality to high radiation tolerant versions. The TSC21020 DSP and 256 Kwords SRAM memory provide a computation power of 20 MIPS/60 MFLOPS. Linking several of these modular boards or extended memory boards (up to 8 Mwords, same format) via one or several of its six IEEE-1355/SpaceWire links can significantly increase this power.

Additional developments have led to even greater integration scale: TSC21020, memory and IEEE-1355/SpaceWire links on a single chip (MCM21020 by Astrium[7]).

COTS based Mini-DPU and Processing Elements

ESA is now developing a COTS based Mini-DPU: a small and radiation tolerant DPU to be manufactured with low cost and highly integrated components.
For small systems, where the volume/mass/power constraint is high (for small spacecraft or modules such as micro-satellites, landers, rovers, robotic arms, etc.), Mini-DPUs based on COTS components can be designed, keeping compatibility with the DSP philosophy and the processing chain based on DPUs and IEEE 1355/SpaceWire links. Indeed, the very high performance and integration level of up-to-date technology components enables to make use of redundancy schemes that compensate the poor tolerance towards space environments of these components. Nevertheless, the main organ of the Mini-DPU, the microprocessor must be as insensitive to radiation as possible, in order to comply with space environment, and this sensitivity must be precisely characterised. This concerns in particular the total dose sensitivity.

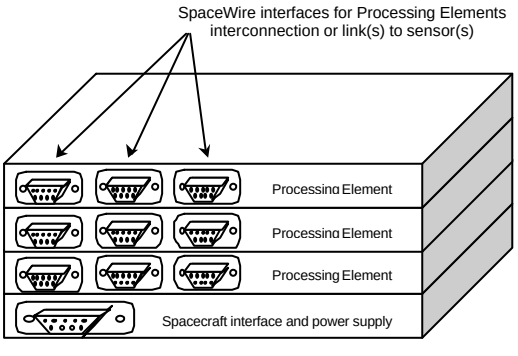


Figure 7

3-level redundant Mini-DPU with 28V/3.3V power converter and spacecraft/low-data-rate interface

To obtain a space compatible system using non space-qualified components, the Mini-DPU system will make use of external redundancy: several Processing Elements connected together can implement redundant schemes (A "Processing Element" is defined here as a DSP microprocessor with potential external memory banks, control logic and high speed serial link interfaces. It is a data processing functional bloc. A Mini-DPU may consist of one or more DSP Processing Element(s). Concept loosely illustrated by Figure 7).

Baseline requirements for a Processing Element

- Processing: in the order of 40 MIPS / 120 MFLOPS when operating in 5 V and 30MIPS / 90 MFLOPS when operating in 3.3 V
- Off-chip memory (EDAC protected): at least 8 Mwords
- idle mode (low power) capability with no data loss
- There shall be at least two Input/Output data interfaces that are compatible with the SpaceWire specification
- Mass: max. 300g
- Volume: max. 160 cm3
- Power supply: 3.3 V or 5 V
- power consumption: 2 W (3.3 V) or 4.5 W (5 V)

IEEE 1355/SpaceWire host interface board

Under ESA contract, 4Links[8] and the University of Dundee[5] have developed a compact PCI interface board for IEEE 1355/SpaceWire communications. The board is based on an SMCS332 chip and so implements 3 IEEE 1355/SpaceWire links. Drivers for MS Windows NT were developed that enable read/write to an IEEE 1355/SpaceWire link up to 70Mbit/s of useful data when the link is set to 100Mbit/s and monitoring of the board.

These boards enable simulation and test in an IEEE 1355/SpaceWire based processing chain (Figure 8).

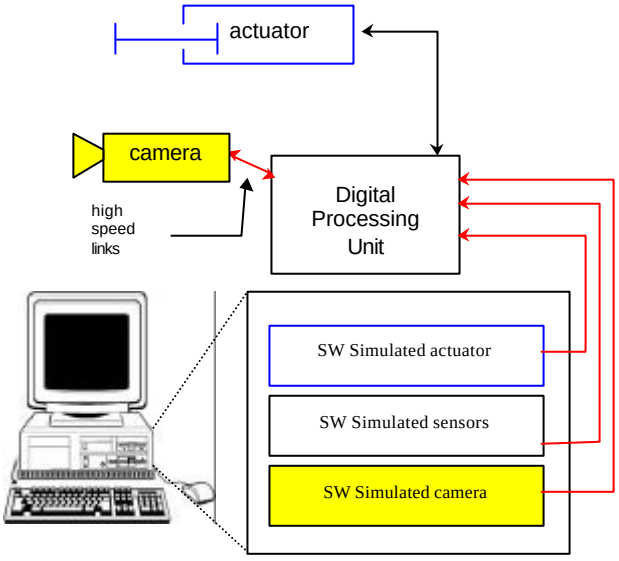
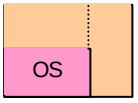


Figure 8 - ***Test of a robotics system***



Real Time Operating System

Growing needs of data processing chains in terms of task scheduling and flexibility lead to an increase of the use of Operating Systems. These Operating Systems must be Real Time, of course, and their use is enabled by the progress achieved in on-board/robotics hardware components (see section Digital Processing Units).

Virtuoso™

ESA has evaluated, chosen, and tuned EONIC[10]'s Virtuoso™ RTOS for use on-board payload systems, and specially DPUs. Virtuoso™ 4.1 is an integrated development environment for hard real-time applications. It supports multi-tasking with a wide range of scheduling options. It also provides a comprehensive suite of development tools that include a project manager, an optimising system generation tool and visual debugging tools. Virtuoso has a multi-level architecture that minimises kernel size, while providing the highest possible processor performance. The Virtuoso™ architecture includes two interrupt-handling levels, a "nanokernel" that manages system level tasks, and a "microkernel" that manages application level tasks.
The evaluation of the scheduling aspects of Virtuoso was made by a third party under an ESA contract (see [RD 9]).
Virtuoso will be flown on METOP and on ROSETTA.

Other solutions

Some missions have hardware or operation constraints such that Virtuoso™ is not suitable. So, ESA is also considering the evaluation of other Real Time Operating Systems for embedded systems, e.g. Open Source ones.

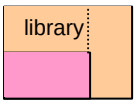


Image processing software library

SSSL[10] is developing, under ESA contract, a software library for on-board image processing. The emphasis is put on functional modularity to achieve both high re-usability and respect of on-board architecture constraints.

Flexible

The Multi-Mission Imager library can handle integer images of pixel depth 1 to 32 bit(s), or 32 float images.
The core of this library should be generic enough to cover most of the basic needs in image processing**,** including some functions to develop robotics application modules, especially on vision capabilities. The proper functional architecture will indeed enable easy later development of additional specific functions.
The core functions are written in ANSI C and defined consistently enough so that some of them may be easily ported to the assembly language of a specific processor. But the C version should already take into account the particularity of embedded systems: little memory, most often divided into local (fast but small) and extended (bigger but slower) memory.

Memory friendly and efficient

The library is written so that only the functions used by the application are compiled and linked. The memory management is left outside of the library so that any hardware configuration where the memory is at least large enough to contain the code of the library itself can run it. The library never allocates any memory but is able to compute and indicate the amount of memory to be allocated for a particular task (this amount is reduced to minimum by pipelining the processing functions of the task). Memory management can then be performed by a separate task which level or safety depends on the user.

The library can run directly on a processor or via a Real Time Operating System (RTOS) in case multi-tasking and pre-emptive scheduling is required (the kernel must be small).

CONCLUSION

The needs in terms of data processing on-board payloads/landers look obviously similar to the ones of the Automation & Robotics field: high processing capabilities for low power, mass, volume and cost. That is why the technology developed for the first is very much reusable in the latter. Communication and synergy between these two domains will lead to better performances and faster achievements.

Reference documents

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More on SpaceWire see: http://www.estec.esa.nl/tech/spacewire/

[RD 5] TSC21020F Data Sheet and further information can be retrieved from:
http://www.atmel-wm.com/upload/doc39a3fb317193b.pdf

[RD 6] Information on the *Mosaic020*-board can be found at:
http://www.dasa.de/dasa/index_e.htm?/dasa/e/dss/technology/technology.htm
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[RD 8] DSP Development (ESTEC Contract No.9736/91/NL/JG, Work Order No.7) – Executive Summary and Technical Report, Issue 1, April 1999.

[RD 9] DSP SW Elements (ESA Contract 12606/97/NL/FM), Summary Report, Austrian Aerospace.

[1] OIP N.V., Westerring 21, B-9700 Oudenaarde, Belgium
[2] FillFactory (formerly IMEC), Kapeldreef 60, B-3001 Leuven, Belgium
[3] IMEC, see FillFacrory [3]
[4] CSEM (Swiss Center for Electronics and Microtechnology)
[5] University of Dundee (UK)
[6] Astrium GmbH (formerly Dornier SatellitenSysteme GmbH, Germany)
[7] Astrium (formerly Matra Marconi Space Toulouse, France)
[8] 4Links (UK)
[9] EONIC (Belgium)
[10] Science Systems (Space) Ltd (UK)