FINDINGS IN DEVELOPMENT OF MINIATURIZED AND DURABLE ELECTRONICS FOR EXTREME TEMPERATURE SHIFTS

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ABSTRACT

This paper delves trough ÅAC Microtecs most resent and past work in the field of miniaturized systems. New data is compared with previous work and provides foundation and validity for the newly developed Thermosonic Assisted Solder Sphere Transfer technique, presented herein.

1. INTRODUCTION

Within advanced space exploration missions there are a need for systems to operate within a large temperature interval. The electronics used for such missions should be able to handle extremely cold environments followed by a drastic increase in temperature. As an example, the mission temperature for a Mars exploration vehicle ranges from as low as -150 °C up to +55 °C.
However, the majority of the advanced space missions currently use temperature controlled zones, e.g. by using heating foils, to obtain less extreme temperature changes. Due to the requirement of continuous heating or cooling of some of the systems on the space crafts or exploration vehicles, the overall power budget is affected in a negative way [2]. An additional negative side effect is the reduced performance for some equipment due to heating. For example, cameras suffer from additional noise levels and sensitivity decreases with increasing temperature, therefore benefitting from operating at a lower temperature.
ÅAC has since many years developed and tested hybrid building techniques suitable for extreme temperature shift applications, due to the good thermal expansion match between silicon and circuit board. The packaging technique has lately been verified on component level, where the hybrid manufacturing techniques have been validated and qualified individually, in accordance with applicable standards for high reliability systems. In addition, an encapsulation technique has been validated, in order to support fully hermetic systems in a miniaturized package.

2. COMPONENTS AND MATERIALS

2.1. Bare Dies

Components with functions necessary for the construction of advanced systems and which are available as bare dies were selected, Table 1.

Table 1 List of bare die components used for flipchip.

Component	Reference	Manufacturer	Space grade/ Space equivalent
SRAM	UT8Q512E	Aeroflex	Space grade
ADC	RHF1401	ST Microelectronics	Space grade
Comparator	LM339	National Semiconductors	Space equivalent
Hex inverter	54AC04 (AC04DIEV2)	ST Microelectronics	Space grade
Op-amp	LM324	National Semiconductors	Space equivalent
CAN Transceiver	TLE6250C	Infineon	Commercial
LVDS /Spacewire	DS90LV019	National Semiconductor	Space equivalent

2.2. Solder spheres

Solder spheres with a composition of 90/10 Pb/Sn were used due to their relatively high initial solidification temperature of 300 °C. The diameter of the spheres was selected to match the pad size and pitch on each respective die, and 110µm and 90µm in diameter were found suitable for the respective die sizes.

2.3. Low Temperature Co-fired Ceramic circuit board

The Low Temperature Co-fired Ceramic (LTCC) circuit boards have internal silver via routing and ENIG finish.

3. MANUFACTURING

Single die chips prepared for traditional wire bonding were Under Bump Metallization (UBM) processed to receive a solderable surface on the chip pads. Solder spheres were placed on the pads and the chips were flipchipped on to the LTCC circuit board. The LTCC were prepared with custom top layer routing and solder mask prior to the flipchip processing. An overview of the manufacturing flow of the miniaturized systems is given in Figure 1.

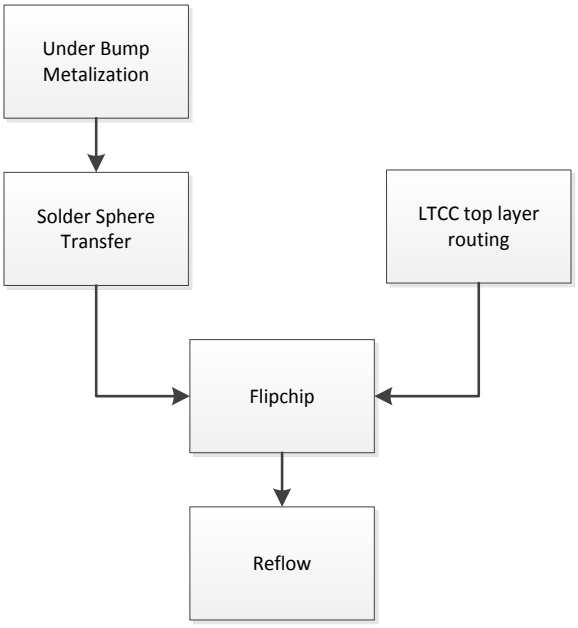

Figure 1 Schematic description of the manufacturing.

3.1. Under Bump Metallization

The (UBM) consists of several wet process steps; cleaning, double zincation, electroless nickel and finally immersion gold. Zinc acts as a seeding layer for nickel, which in turn creates a solderable surface and diffusion barrier. The finishing gold layer prevents oxidation of nickel and provides a surface more suitable for soldering. The layer thickness are approximately zinc <1 µm, nickel 5 µm and gold 100 nm, respectively.
Since the chips have different pad materials ranging from pure sputtered or evaporated aluminium to aluminium doped with copper and silicon of various grade, comprehensive development was required to optimize and limit the number of processing techniques for all the chips, so that the process could be suitable for a large range of single die chips and make production of systems feasible.

3.2. Flux free Solder Sphere Transfer

Solder sphere transfer were conducted on chips after inspection of the UBM process. For evaluation purposes chips with poorer UBM quality and lower likelihood of successful soldering were processed with solder spheres as well, in order to create a knowledge foundation and guidelines on how to grade UMB quality, as pass or fail.
Two types of flux free solder sphere transfer techniques have been used, solder jetting and ÅACs own novel Thermosonic Assisted Solder Sphere Transfer (TASST), which can be applied to single die chips.
The TASST method, Figure 2, comprises a few simple steps. Initially the solder sphere is picked up using a placing tool and aligned over the pad. Subsequently the sphere is pushed down using ultrasonic oscillation while heating, and it becomes firmly attached to the pad.

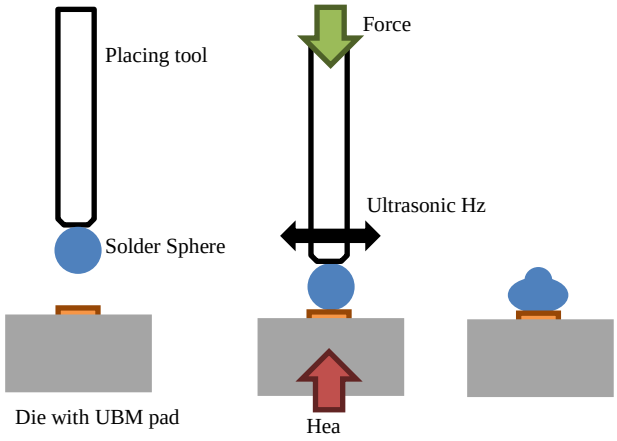

Figure 2 Schematic description of Thermosonic Assisted Solder Sphere Transfer

All dies were reflowed after TASST in low pressure formic acid atmosphere, allowing the deformed solder spheres to regain their shape and self-align on the pads, Figure 3. No reflow was performed on the dies with solder jetted bumps prior to the flipchip process.

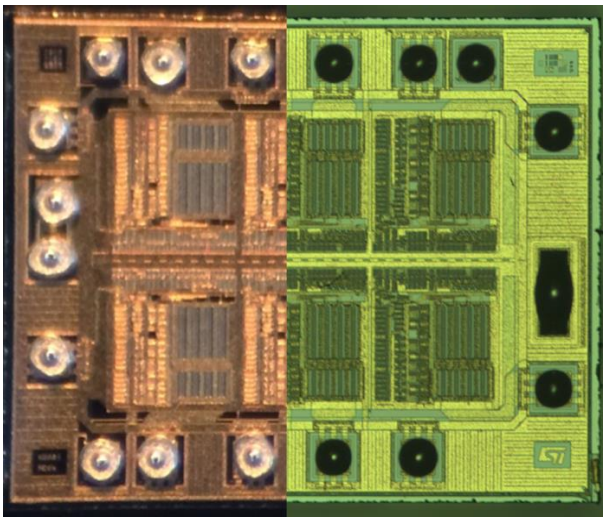

Figure 3 The 54AC04 single die after TASST (left) and after reflow (right)

3.3. LTCC top layer routing

LTCC boards with several layers of internal routing were prepared with top layer copper routing, which connects the LTCC vias with solder pads on the dies. The top layer had ENIG or ENEPIG finish and a BCB solder mask. Post fired LTCC boards were procured from a sub supplier.

3.4. Flipchip

The bumped dies where flipchipped with custom parameters depending on the die size and number of

bumps. The load and heat parameters have been developed through thorough testing and development.

3.5. Reflow

The flipchip was performed in a flux free reflow low pressure formic acid atmosphere. The temperature ramping scheme was carefully selected, in order to form a bump bond/interface that withstands mechanical and thermal stress.

4. TESTING

4.1. Inspection

As a standard production step for evaluation ocular inspection was performed. While inspecting the outcome of the different processes a library of observations were established in order to build a foundation for evaluation, enabling an increase in yield by more accurate selection of approved parts before assembly.

4.2. Bump shear test

After solder sphere transfer, bump shear testing was performed on several dies according to the JESD22-B117A standard in a Dage 4000 shear test equipment.

4.3. Thermal cycling

Two different thermal cycling tests have been performed on miniaturized systems build with the ÅAC technique. One test, that was performed according to ECSS-Q-ST-60-05C, Table 2, had a rapid temperature change in a relatively high temperature interval. The other test was performed in a low temperature interval with reference to the Exomars rover and Mars environment [1], Table 4. The new TASST method has not yet been evaluated using thermal cycling.

Table 2 Parameters for rapid temperature change and high temperature cycling.

Parameter	Value
Cold temperature	-55 (+0/-10)℃
Hot temperature	+125 (+15/-0)℃
Dwell time	≥ 10 minutes
Temperature gradient	≤ 12 ˚C/min
Number of cycles	100
Atmosphere	Air

Table 3 Parameters for low temperature cycling.

Parameter	Value
Cold temperature	-135 (+0/-5)℃
Hot temperature	+55 (+5/-0)℃
Dwell time	≥ 1 minutes
Temperature gradient	≤ 3 ˚C/min
Number of cycles	40
Atmosphere	8 mbar

5. RESULTS

Bump shear testing doesn't show any significant differences in shear strength between the two used methods, Table 4.

Table 4 Bump shear results for solder jetting and TASST.

Chip type	Method	Avg. max. shear force (g)	Std. Dev (g)
LM324	Solder jetting	27,9	4,8
LM324	TASST	27,8	2,0
LM339	Solder jetting	25,6	4,6
LM339	TASST	28,2	2,1
DS90LV019	Solder jetting	36,0	2,9
DS90LV019	TASST	30,8	4,0
TLE6250C	Solder jetting	32,4	4,3
TLE6250C	TASST	34,4	2,9
54AC04	Solder jetting	30,2	2,5
54AC04	TASST	28,7	1,8
UT8Q512E	Solder jetting	28,2	6,0
UT8Q512E	TASST	30,5	4,7

During the development is was noted that the TASST method had fewer failure modes relative to the solder jetted dies, thereby increasing the yield of solder sphere transfer. It was also noted that TASST had higher success rate on slightly discoloured and rougher UBM pads, allowing more dies to pass the UBM process.

It was noted that a system built using ÅAC processes had high probability to perform well during and after the preformed temperature testing [1].

6. CONCLUSIVE DISCUSSION

Solder jetted dies and TASST prepared dies show no significant difference in the performed shear tests, indicating that the TASST method is suitable for bumping of dies, however further environmental testing is needed.

To visualise the benefits of miniaturization, three daisy chain circuit boards with the same component was built, Figure 4. The component was an operational amplifier, LM324, available in a variety of packages as well as bare die and as space qualified component. The standard packages were mounted on standard PCB with standard design rules. The bare die was UMB processed, bumped with ÅACs TASST method and flipchip mounted on a LTCC circuit board. Besides the obvious size difference the miniaturized units also provided the possibility of increased operation temperature range.

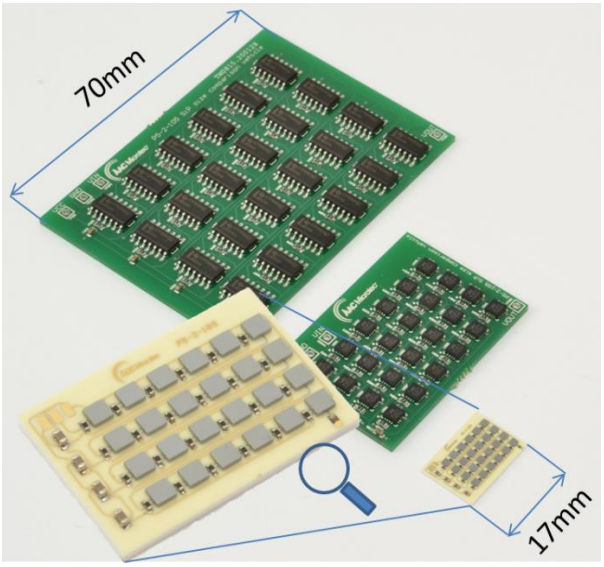

Figure 4 Size demonstration of miniaturization. Top-left: 14 SOIC components. Middle: 16 QFN components. Bottom-right and magnified insert: Flipchipped bare dies.

7. FUTURE WORK

ÅAC plan to investigate if other metal systems could be used with the TASST method. Solder spheres of smaller and larger sizes are also of interest, and the possibility to initiate such an activity is currently under investigation.

A project supported by ESA, together with Swedish and Swiss companies, aiming at a motor controller for extreme environments is expected to start during 2015.

8. ACKNOWLEDGMENT

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9. REFERENCES

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