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Development of SIS - Satellite controller Integrated with Star sensors -

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ABSTRACT

SIS is a Satellite controller Integrated with Star sensors, which has been developed as a prototype model of a compact, low-cost satellite controller. SIS integrates attitude sensors into a star sensor and integrates several electronics for star identification, attitude determination, attitude control, and data handling into a single processing unit. SIS meets high reliability requirements by adopting a modified voting system even though it employs high performance commercial parts to increase the calculation speed. Consequently, we can drastically decrease the size and cost of the satellite controller. SIS will be included in the payload of the SERVIS-1 satellite scheduled for launch at the end of this year.

1. INTRODUCTION

Cost reduction has become one of the most important requirements in recent space projects. In particular, to increase the ability of many users to take advantage of the space environment for various purposes, it is necessary to reduce the price of satellites and to increase available payload space. To realize this objective, we have been developing a prototype model of a compact and low-cost satellite controller, SIS (Satellite controller Integrated with Star sensors) (Fig. 1)

SIS employs high-performance commercial parts to improve the calculation speed, and it enables the following approaches to meet the requirements of cost and weight reduction.

Fig.1 SIS Flight Model

(1) Integrating earth sensors, sun sensors and gyroscope into a single star sensor

(2) Integrating electronics for sensor data processing, attitude control, and communication data handling into a single processor unit

While employing commercial parts is good for cost reduction, it may decrease the reliability. We maintain high reliability by developing a modified voting system with four-CPUs and four-CCDs and installing the commercial parts into a metal shield case.

We have already completed development of the SIS flight model and have undertaken the performance and environmental tests at the component level. Currently it is undergoing system interface tests. SIS will be launched as part of the payloads of the SERVIS-1 satellite [1] at the end of this year.

This paper describes the main features and the configuration of SIS.

2. MAIN FEATURES

2.1 Integration of Attitude Sensors and Electronics

Figure 2(a) illustrates an example of conventional satellite controllers. In principle, a star sensor alone determines a satellite's exact attitude. However, because numerous calculations are required to extract star images in the field of view and the pattern that corresponds to the star database, it is difficult to calculate the attitude in a reasonably short time by using a star sensor alone. Multiple attitude sensors and an additional processing circuit are also needed. Therefore, we have increased the processing system's efficiency by adopting high-performance commercial ICs and developing a compact image preprocessing logic installed in FPGA. Consequently, the following approach to cost-reduction could be realized.

(1) Integrating all attitude sensors into a single star sensor

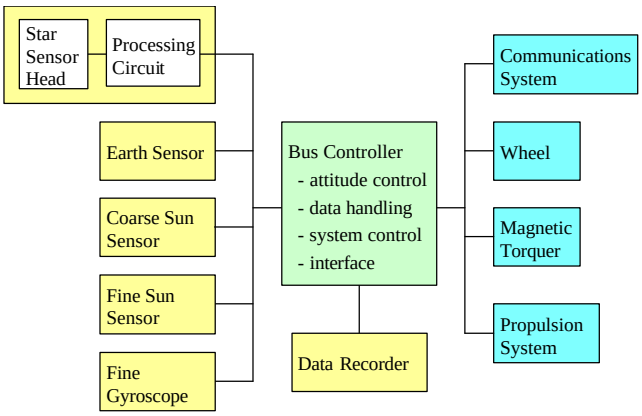
(2) Integrating multiple electronics into a processing unit.

As a result, we have realized a satellite controller with a simple configuration, as shown in Fig. 2(b).

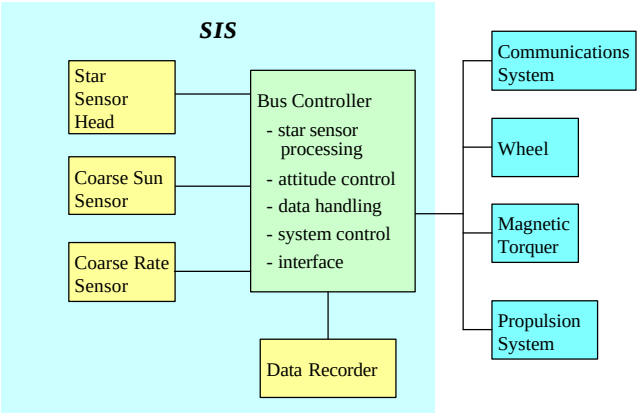
For preprocessing star images, we adopted the method in which FPGA calculates the local maximum of brightness, which indicates the approximate position of the star image.

A coarse sun sensor and a coarse rate sensor have also been installed in the configuration. The rate sensor is used only for initial rate dumping just after the release from the rocket, while the sun sensor is used only in safety mode. These sensors are not obstacles because they detect rough attitude and rate, and they are very lightweight and very low-cost.

As shown in Table 1, commercial CPU, CCD, SDRAM, and E^2PROM are employed to reduce the system's cost.



(a) Typical example of conventional satellite controller



(b) Implementation of SIS

Fig.2 Comparison of implementation

Table 1. Commercial parts adopted for the SIS

Description	Qty	Spec.	Use	Radiation Tolerance
CPU	4	32bit RISC	sensor signal processing, attitude determination and control, data handling, satellite management	500Gy(Si)
CCD	4	330K pixel	attitude identification	proton 20Gy(Si)
SDRAM	8	256Mbit	data recorder	50Gy(Si)
E^2PROM	8	1Mbit	program memory	20Gy(Si)

2.2 Highly Reliable Architecture

Although employing commercial parts is effective for cost reduction, reliability may be lost if highly reliable space parts are simply replaced by commercial ones. To overcome this obstacle, we have developed the modified voting system, which is composed of a hierarchical combination of four CPU modules with commercial CPUs and CCDs, and a supervisory control unit (SCU) with high reliable FPGA. The system's concept is illustrated in Fig. 3.

Fixed star images captured by the four separate sensor heads are first processed by each sensor's own CPU. The detected fixed star data is then shared by the four CPUs, and the four CPUs similarly calculate the attitude and attitude control commands. Finally, the voting system picks up the harmonized data by comparing the calculation results each other. By adopting this architecture, the CPU malfunctions due to radiation-induced memory upsets are eliminated, thus a high degree of reliability is provided.

The SCU program code is installed in the four E^2PROMs, and fetched through the voting system; therefore SCU operation is insusceptible to radiation. In addition, SCU performs the following operations: controlling the power to the CPU modules, monitoring the number of CPU malfunctions, CPU initialization, and sharing data between the CPU modules.

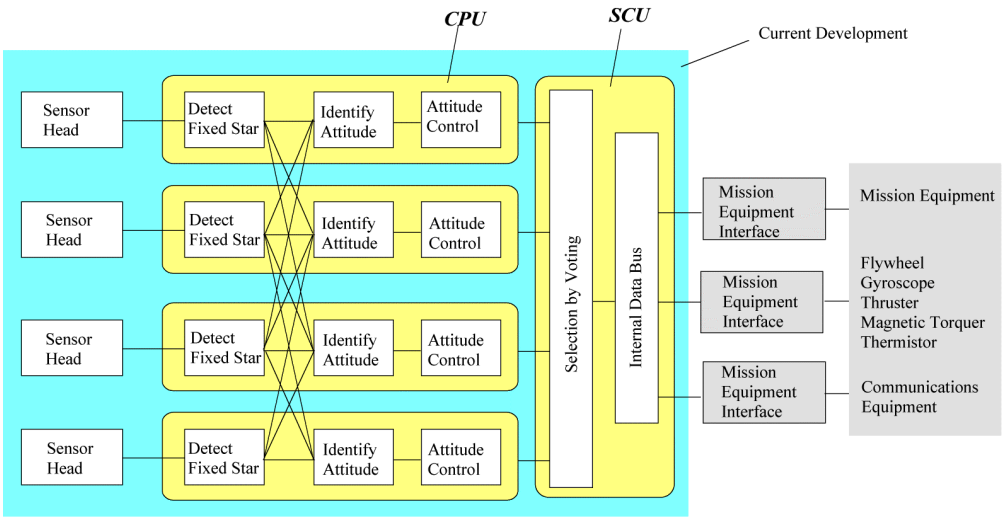


Fig.3 Block diagram of processor unit

2.3 CPU Module

The CPU, SRAM, E^2PROM *et al.* are sealed in a metal case, which is called a CPU module. Its schematic structure is shown in Fig.4. It improves the system's cooling capability, radiation tolerance and structural reliability.

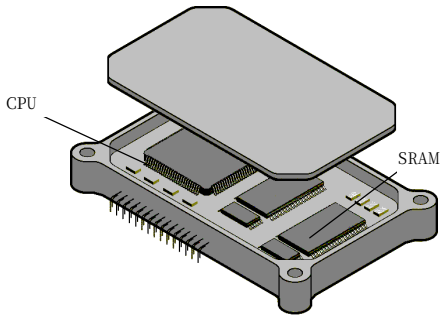


Fig.4 Schematic structure of the CPU module

3. CONFIGURATION AND DETAILS

3.1 SIS Architecture

Figure 5 shows the SIS architecture. The main specifications are given in Table 2.

The SIS consists of the following components:

(1) SISE
- Processor section
- Data Handling section
- Data Recorder section
- Power Supply section

(2) SISH

(3) SISS

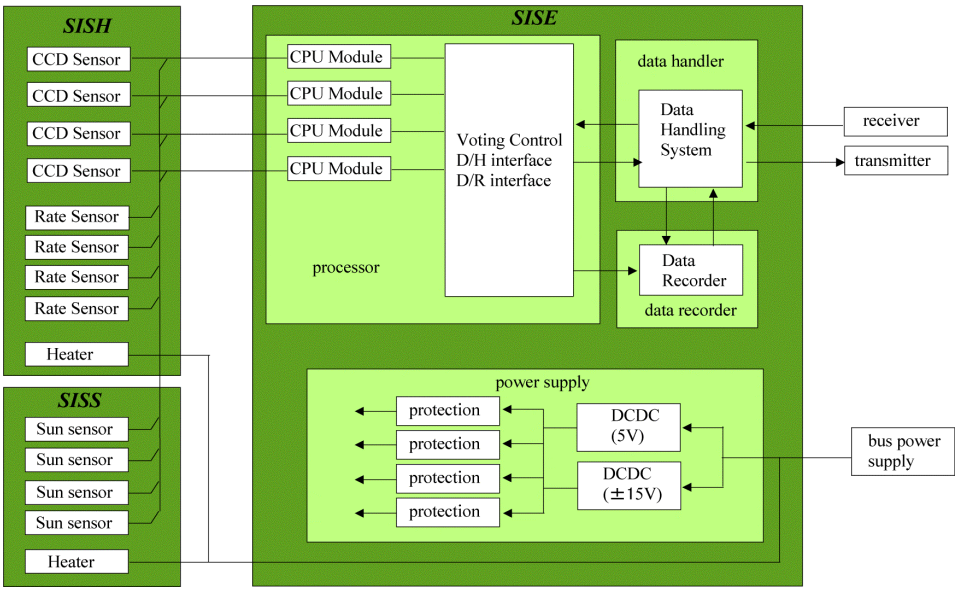


Fig.5 Block diagram of SIS

Table 2. SIS Performance

Category	Item	Performance
Attitude determination function	Star detecting sensitivity	Visual magnitude of Mv=+5 detectable
	Attitude determination accuracy	+/- 0.02 deg in each axis (referred to inertial space)
	Attitude rate detecting accuracy	0.1 arcmin/sec in each axis
Attitude control function	Attitude control accuracy	0.1 deg in each axis
	Sampling period	125 msec
Data handling function	Throughput capacity	3-channel packets of TLM & CMD each (extendable)
Data recorder function	Memory size	1 Gbit (BOL)
	Error correction ability	2 bit per 1 byte detectable 1 bit per 1 byte correctable
Rate detecting function of inner rate sensors	Rate detection range	+/- 1 deg/sec (extendable)
	Rate resolution	+/- 0.01 deg/sec
Sun direction detecting function by SISS	Detection range	+/- 60 deg
	Detection accuracy	+/- 3 deg
Size (excluding projection)	SISE	252 x 320 x 103 mm
	SISH	489 x 489 x 249 mm
	SISS	130 x 47 mm (Diameter x Height)
Weight (excluding harness)	SISE	8 kg
	SISH	7.9 kg
	SISS	0.5 kg
Power consumption	Nominal mode	45 W (typical)

3.2 SISE

Processor section

This consists of the aforementioned CPU module and an SCU. The external inputs/outputs of this section consist of a data bus system.

A block diagram of a CPU module is shown in Fig.6. The CPU, SRAM, VRAM, E^2PROM, and FPGA are mounted. All the external interfaces are executed through the FPGA. Preprocessing logic of captured images is also installed in this FPGA.

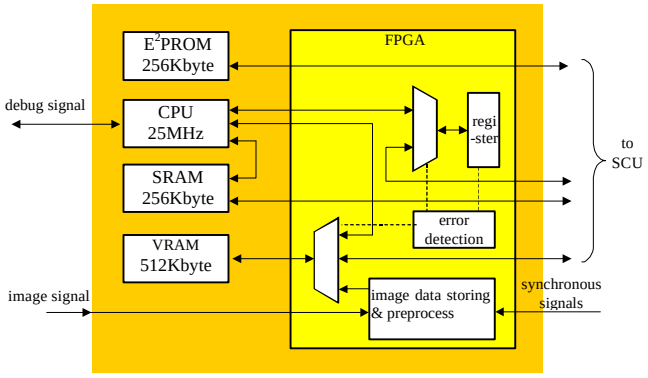


Fig.6 Block diagram of CPU module

Data Handling section

This section sends and receives data using the serial communication lines. Immediately after it receives 1-byte data, it writes the data in the CPU modules, and just before it sends 1-word data, it loads the data from the CPU module. This minimizes the need for buffer memory. It also has a function to decode and execute several commands such as power on/off by only using hardware logic.

Data Recorder section

SIS contains a data recording function to store the telemetry data of mission components. We adopted a commercial-use SDRAM with a large capacity as the memory device. Table 3 shows the recorder's specifications.

There is a possibility that the data may change and the memory cells may be permanently damaged by radiation while the satellite is in orbit. The recorder checks every cell in the background. If it detects 1-bit error, it corrects the error. If it detects a permanent error, it excludes the bank with the error, which is a 1-Mbyte block of memory. The hardware cooperates with the CPU software. The CPU software records the relevant NG bank number(s) and shows it to the hardware. According to this information, the hardware will operate using only good banks without containing a large scale of mechanism to detect and exclude the NG bank(s).

Table 3. Specifications of the Data Recorder

Characteristic	Value
Recording system	FIFO (First In First Out) memory system
Memory size	Gross : 2Gbit Net : 1Gbit Comprises 8 chips of 256MbitSDRAM
Reliability of data	2 bits error per 8 bits detection, 1 bit error per 8 bits correction (the function based on extended hamming code system) Background error detection and correction Excluding NG bank
Signal interface	3-line serial communication (In/Out)
Control interface	16 bit parallel I/O bus
Control signals	transiting mode, selecting bank
Status	Full, Empty, Bit error occurrence recording/playing bank

Power Supply section

Because commercial parts are employed, protection from latch-up induced by radiation is vital. Though all commercial parts employed here have high radiation tolerance, a safety function to protect against overcurrent is provided.

3.3 Sensor Head (SISH)

SISH is equipped with four CCD cameras and four rate sensors.

The camera detects stars brighter than a visual magnitude of Mv = +5 in a wide field of view of 13x13 degrees. To avoid visual interference due to stray light with incident angles of over 35 degrees from the sun or the earth, it is necessary for the camera to have a baffling system that usually increases the size of the optical system. We applied two unique light shielding techniques and realized a small baffle length of 140 mm [2]. The

techniques are the application of the total internal reflection phenomenon inside a nearly-hemispherical convex lens and the use of gloss black paint. Figure 7 shows the baffling system. We confirmed the performance of the stray light attenuation system in the ground test.

A vibratory type space-proven gyroscope has been adopted for the internal rate sensors. The sensors are employed to detect angular rates exceeding the star sensor's limits.

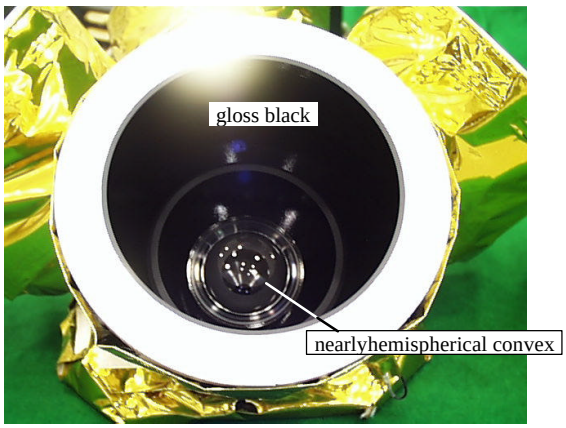


Fig.7 Picture of the baffling system

3.4 Coarse Sun Sensor (SISS)

SISS is utilized as a backup sensor in safety mode.

SISS has a simple structure in which four photo-diodes are fixed inside four glass windows, as shown in Fig.1. Using the photo-diodes' output levels, the sun's direction can be determined to an accuracy of 3 degrees in the measuring range of the almost-hemisphere.

3.5 Onboard Software

Onboard SIS software consists of one system for the CPUs and one for the SCU, both of which are stored in the E^2PROM in all CPU modules.

We have improved the reliability of the star identification process by using several continuous sensor images instead of requiring higher optical system accuracy [3].

4. DEVELOPMENT STATUS

The SIS Flight Model has been already manufactured, and it has been confirmed that attitude control procedures can be executed within 8 Hz by functional tests. It has been also confirmed that the SCU can detect errors in CPU modules and continue normal operation by a test that simulates the error occurrence in a CPU module due to radiation. Furthermore, we verified its compatibility with the environment of space via vibration and thermal vacuum tests.

At present, it is installed in the satellite and is undergoing various interface tests.

After being launched in autumn of 2003, the system will undergo a series of tests in orbit to evaluate the following functions: image capturing, attitude determination, data processing, attitude control and unnamed others.

5. SUMMARY

We have developed an SIS - Satellite controller Integrated Star sensor as a prototype of a future satellite controller that reduces the size and cost of the satellite bus. SIS enhances processing ability by using high-performance commercial parts, and enables the integration of several types of attitude sensors into the star sensor, and also integrates various data processors.

The flight model has been manufactured, and the effectiveness of its architecture has been confirmed in ground tests. SIS will be appraised in orbit as a mission component of SERVIS. In the future, we plan to upgrade SIS's reliability sufficiently for bus component use, and make it a finished product.

ACKNOWLEDGEMENT

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Thanks to the entire SIS team for their help.

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