RECONFIGURABLE TECHNOLOGIES FOR SPACE ROBOTICS

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ABSTRACT

Space robotic systems offer several advantages to the standard all-electronic approach and are aimed to tackle more advanced tasks in orbit. The sensing capabilities of the robotic systems are critical to provide accurate measurements to the control algorithms. Likewise, the processing algorithms need to have increasingly processing power to fuse all the sensors provided information and to provide an accurate control on the final system. The problem is that the more amount of information is provided by the sensors the greater the processing capacity that is needed. The increasing processing power of new space qualified processors and the new generation of reconfigurable FPGAs promises to fill this gap.

1 INTRODUCTION

Current scientific and earth observation missions (i.e. Meteosat Third Generation, Copernicus programme, PLATO, JUICE, EXOMARS) pack on board a wide set of complex processing algorithms such as interferometry calculations, centroiding, filtering or image enhancement, but all of them share three main characteristics:

- These algorithms are static. Of course they can be reconfigured through Tracking, Telemetry and Control (TTC) systems from earth but they remain constant between SW updates, and process data in a fixed way, independently of the environment of the satellite and, most importantly, independent of the content and quality of the acquired image.
- These algorithms are targeted to improve the image quality or to reduce its volume to ease transmission to ground but in no case are targeted to extract scientific information on the satellite, the extraction of scientific information is fully performed on earth after the reception of the images.
- As no scientific information is extracted on board, all the mission related decisions are taken on the ground. No autonomous decisions related to the science observations are taken on the satellite other than following a pre-fixed If-then sequence for very obvious failure modes.

Beyond this present state of the art, new space robotics can answer the needs of such systems as are aimed to provide a platform that will allow in-flight dynamic reconfiguration to provide adaptability to the mission embarked algorithms. In this way, the instrument algorithms will be modified in real time to respond to changes in the incoming data as well as in changes in the instrument environment. This will allow the instrument to optimize its performances autonomously and increase its resilience to external factors through the duration of the mission.

By using reconfigurable robotic platforms, the instrument algorithms will be modified in real time to respond to changes in the instrument data as well as in changes in the instrument environment. This will allow the instrument to optimize its performances autonomously and increase its resilience to external factors through the duration of the mission. This adaptability shall take the form of an intelligent agent implemented inside the space system processing platform and able to react to the instrument environment as well as to respond to high level instructions.

A key element of the payload of future robotic systems are architectures where processing can be parallelized. This could be a many-core based on-board digital signal processor implemented on either space qualified devices or reconfigurable FPGAs. Such systems would need to include a cross-layer fault management technology, enhanced autonomy and advanced data processing software. The target is to boost the data quality on board, as well as to preprocess and compress the instrument data thus reducing the amount of information to be transmitted to ground. This would allow the usage of larger sensors in a low

cost platform maintaining the performance of current bigger solutions.

In this paper we present a survey of possible Processor and FPGA based reconfigurable platforms that are aimed to be used in space robotics, together with a an introduction of a use-case where both instrument control and on-board data processing is implemented in parallel. The paper is organized in the following manner: Section 2 introduces a survey of current Processor / FPGA-based architectures, analyzing their performance as well as their adequacy to the space environment; Section 3 introduces the needs of future architectures for the next generation Processors / FPGAs. Section 4 briefly describes a possible use-case architecture, including its subsystems and interfaces; and finally Section 5 concludes this paper, providing conclusions and laying out directions for future work.

2 PROCESSING ARCHITECTURES FOR SPACE ROBOTICS

The architectures surveyed are targeted at the implementation of adaptive robotic algorithms focusing Instrument Control Units or On-Board Computers of a Space equipment.

This target is appropriate for both the immediate implementation on Space Grade FPGAs or in the conventional way of producing space-grade microprocessors, using hardened ASIC technology platforms.

This section discusses the current state-of-the-art and its application in the space of both technologies.

2.1 Space Grade Microprocessors

There are several European space-qualified microprocessors today and their market is growing more and more.

The ATMEL ERC32 was the first European 32-bit space microprocessor. Introduced in the mid-1990s it first existed as a three-chip solution. These three devices where then merged into one device consisting of a processor pipeline, caches and a memory controller.

ATMEL AT697F consists of a processor with UART, PCI and simple GPIO interfaces. While this provides a generic processor, the avionics integration typically requires multiple support FPGAs to be included in the system to provide interfaces for buses such as TM/TC, SpaceWire and MIL-STD-1553B as well as for additional UARTs.

Cobham Gaisler GR712RC is a dual-core processor provides additional interfaces (MIL-STD-1553B, Ethernet, TM/TC, additional UARTs, SPI, I2C) compared to the AT697F.

The Cobham Gaisler GR740 is the most recent and most powerful processor. The device provides several external interfaces (Gigabit Ethernet, MIL-STD-1553B, SpaceWire and parallel PCI) and has a wider memory interface compared to the earlier generation processors to support higher bandwidth and a higher amount of external memory using existing space-grade memory devices. The device currently exists implemented on radiation hardened technology with the first devices for space missions being delivered in the first half of 2018.

Processing capabilities will extend the current state-of-the-art through the introduction of clusters of processors interconnected by a network-on-chip system also capable of supporting dedicated acceleration cores.

The Scalable Sensor Data Processor (SSDP) is a next-generation mixed-signal ASIC which embedds in the same package two Xentium Digital Signal Processors (DSPs) together with a LEON3FT General Purpose Processor (GPP) [1]. Such integration provides a heterogeneous multiprocessor System-on-a-Chip (SoC), capable of performing not only processing-intensive tasks, but also control tasks.

Looking at the worldwide space market, the main competitor available today for the European GR712RC and GR740 devices are the RAD750 device from BAE Systems (US) and the SCS750 board from Maxwell (US). Both are based on PowerPC750 devices. A goal for the GR740 development was to provide a European alternative to RAD750 and the Maxwell board. One particular mission that was forced to use US components due to lack of a European alternative was GAIA (Global Astrometric Interferometer for Astrophysics, ESA mission for space observation). Studies have now shown that the GR740 provides enough performance to replace the PowerPC processors in the GAIA application .

Another competitor is RAD5545 from BAE systems (US). This device is based on a commercial quad-core PowerPC architecture and features SpaceWire, PCI, RapidIO and additional low-speed interfaces. The device outperforms both existing and announced European developments, however the availability of this processor outside the US remains uncertain.

NASA, with interest from the Air Force Research Lab (AFRL), has determined the need for High Performance Spaceflight Computing (HPSC) for multiple mission applications associated with

robotic science investigations, other remote sensing, and human space exploration. The proposed architecture is an octo-core using commercial processor IP. This processor has a performance requirement of 15 gigaoperations per second (Gops). The contract for this processor development has been awarded to Boeing (US) and it is currently unknown what the final architecture and processing capability will be.

Boeing Corporation has announced several test devices on small geometries. Several of these are microcontroller like systems that are based on single-core ARM processors. No commercialization attempts are known and the implementations have instead been targeted at showcasing US ASIC technology developments.

The H2020 DAHLIA [2] project is developing a Very High Performance SoC based on STMicroelectonics European 28nm FDSOI technology with multi-core ARM processors for real-time applications. The projected performance improvement over the state-of-the-art GR740 is 2-3x the processing capability.

The RC64 device from Ramon Chips (Israel) is a many-core device with 64 GPP/DSP cores capable of 100 Gops or 12 giga instructions per second (Gips). This device far outperforms all known European and US developments in terms of processing power. Of the developments listed as beyond the state-of-the-art this is also the one that has progressed the most with prototype devices already available.

2.2 FPGA Based Technologies

Currently the high capacity FPGAs available for space usage are the Xilinx XQR5VFX130 bulk CMOS 65 nm SRAM based FPGA and the MICROSEMI RT4G150 bulk CMOS 65 nm Flash based FPGA.

The Xilinx XQR5VFX130 is an SRAM based FPGA with the key advantage of being reprogrammable and thus the configured design can be modified, even during fly operations.

Main issue for SRAM based FPGAs for space applications is that configuration memory can be corrupted due to radiation effects leading to the operation interruption of the FPGA (SEFI event that stands for Single Event Functional Interrupt). However, this FPGA is a Radiation Hardened component where the critical internal elements have been protected against radiation effects.

This FPGA has Space heritage being flown, or selected, for the following missions:

- Iridium Next
- Orion Multi-Purpose Crew Vehicle
- Taiwan Imaging Satellite
- OSIRIS-Rex
- Laser Comm. & Relay Demonstration (LCRD)
- Heinrich & Hertz (H2) Satellite
- NovaSAR
- Glonass-K GPS
- Grace Follow-On

Flash based FPGA does not present configuration memory corruption issues, as it's the case for SRAM based FPGAs. In addition this FPGA is a Radiation Hardened component where the internal elements have been protected against radiation effects. An example of a space Flash based FPGA is the MICROSEMI RT4G150 bulk CMOS 65 nm.

The main drawback for these FPGAs is that, although in flight reconfiguration is theoretically possible, it's not recommended due to potential destructive effects, if radiation effects occur during programming of the device.

NanoXplore in collaboration with ST-Microelectronics is developing the BRAVE FPGA family with a medium FPGA already prototyped and a large one still on-going. The goal of this activity is to produce the NanoXplore NX1H140 bulk CMOS 65 nm SRAM based FPGA.

At the end of 2015 ALTERA announced plans for the Space qualification of one of the parts of the Stratix V family, the 5SGXMA7H2F35C2 device. Since then no further information has been received.

At the beginning of 2016 XILINX announced plans for the Space qualification of one of the parts of the UltraScale Plus (ZU+) family, the RT-ZU19EG device [3]. After some tests, the ZU+ component was discarded for its qualification and the new Xilinx target devices has been moved towards a Kintex Ultrascale 60 [4]

NanoXplore is also performed some design activities to extend the BRAVE RH FPGA to the 28 nm technological node, based on the ST-Microelectronics FD-SOI process, in what is called NG-Ultra FPGA family with prototyping of the NX2H550 foreseen by 2019. These tests are also in the context of the H2020 DAHLIA [2] project

3 BEYOND THE STATE OF THE ART

Space missions, especially the long lasting autonomous missions, require fault-resilience in order to provide graceful degradation capabilities for the spacecraft. Rad-hard components are not only expensive but there is a lack of the hardened counterparts for newer technologies and more efficient (e.g. multi-/many-core) architectures. However, applying COTS IC and FPGA technologies requires protection mechanisms at different layers of the on-board computing system. While the software layer has been thoroughly addressed by the existing state-of-the-art, there is a shortage of truly cross-layer approaches as well as standardized solutions for HW-layer fault management.

Today, on-chip health monitoring solutions for SoCs are still at their infancy stage. Pilot prototypes (including e.g. ESA activity T201-005ED) are lacking a systematic approach probing several ad-hoc ideas. For higher-level systems (off-chip), there exist domain-specific health-awareness and fault management techniques such as S.M.A.R.T. (Self-Monitoring Analysis and Reporting Technology) in computer devices.

The range of ESA actions that contribute to at least coarse-grain health-awareness is currently also very limited. The recent activity that is most closely related here is Standard Platform for Monitoring (SPMON2) (G617-195GI) [5]. According to the authors, the main benefit is that it is a generic system easily configurable to any type of mission (e.g. SWARM, Sentinel, Bepi Colombo, EXOMARS, Euclid, etc.) and flexible enough to also monitor and control similar Data Systems (e.g. Flight Dynamics Systems, ESTRACK Management System).

The SPMON technique is operating off-chip, at a higher level with respect to SoC, and requires a sub-system that collects fine-grain health and status data from cores and modules inside the SoC. A systematic approach to this challenge is missing today.

There are, however, some isolated activities at ESA, targeting low-level data collection, but orchestration and general strategy are currently missing. In this context, it is worth mentioning the following two actions: Microcontroller Softcore for Space Applications (G617-251ED) [5] and Network on Chip (NoC) for many-core System on Chip in Space applications (T201-005ED) [6]

The first one lists “high priority interrupt on parity error in order to signal the fault to the application” activity as a part of the development plan. The second one, among other project activities, targets “graceful degradation mechanisms” based on sensor data processing. None of the two projects targets the ability to simultaneously collect and process data from dozens or even hundreds of on-chip sensors or parity checkers, which is the key to a successful SoC-level Health-Awareness.

Activities targeting system health are called Failure Detection Isolation and Recovery (FDIR). Most of them are performed at the software level (application), involve high-level system modelling and embrace the complete satellite functionality. An example activity is given below [7]. This activity, according to authors, is contributing to mitigation of “the current lack of systematic approach and the lack of engineering transparency and guidance of the FDIR engineering process, with also the aim to decrease overall complexity.” It is neither focusing on SoC level fine-grain FDIR nor addressing permanent faults or a damage.

Finally and directly linked with space robotics, the PERASPERA [8] action, as part of the “Space Robotics Technologies” Strategic Research Cluster (SRC) in Horizon 2020, has the goal of enabling major advances in strategic key-points of Space Robotics Technologies, in order to improve the European competitiveness.

The main objective of this cluster is the creation, within the 2020-2030 timeframe, of the necessary tools to ensure and consolidate the maturity of the Space Robotic technologies for orbital maintenance missions and planetary exploration. These activities are developed in coherence with the existing and planned developments at national, commercial and ESA level.

In this context, the 2016 Space H2020 on Space Robotics Technologies (COMPET-4-2016) has launched 6 different Operation Grants to enable the competitiveness in strategic key-points of Space Robotics Technologies.

- (OG1) European Space Robot Control Operating System: ESROCOS
- (OG2) European Robotic Goal-Oriented Autonomous Controller: ERGO
- (OG3) Infusing Data Fusion in Space Robotics: InFuse
- (OG4) Integrated 3D Sensors suite: I3DS
- (OG5) Standard Interface for Robotic Manipulation of Payloads in Future Space Missions: SIROM

- (OG6) Facilities for testing orbital and surface robotics building blocks: FACILITATORS

4 THE I3DS USE CASE

Integrated 3D Sensors (I3DS) [9] is a project co-funded under H2020 and the SRC as the Operational Grant n°4 of the programme Support Activity" (PSA) under PERASPERA.

I3DS is the only Operational Grant under the PERASPERA action that targets the development of suitable actual HW for space robotics on the contrary of the other 5 OGs that are focused on high level architectures, software or robotic algorithms. I3DS is therefore focused both in the development of space sensors and processing architectures for their use in future space missions.

From the very beginning it is important to focus on HW technologies that may be used in an space environment; otherwise the designed robotic algorithms and software may not fit a real target. If not, the design of algorithms and software architectures that are correctly working in standard COTS computers may not properly work when adapted to a Space HW.

Typically, Space HW does not have as much resources (memory, processing capabilities…) as ground computers. This is a huge limitation as it is necessary to adapt and optimize all the software and developed frameworks to be included in a Space platform. Simulations and algorithms perfectly working in ground standard COTS computers may not work properly in space HW and it would be necessary to adapt the functionalities to the space target and in last instance to dismiss some functionalities.

Therefore, targeting algorithm implementations into platforms and architectures that are compatible with the space ones, will lead to a future successful implementation, otherwise final implementation on an space target may not comply with the expectations. In this sense, the I3DS project has been focused on using compatible space targets to implement the sensor processing algorithms and demonstrate a real use case.

2.2 The I3DS ICU

I3DS provides an abstraction of the many electrical interfaces of different sensors by centralizing the data flow using dedicated communication nodes. All the data acquired from the sensors is centralized in an Instrument Control Unit (ICU) that is in charge both of controlling the different sensors and pre-processing the data for later delivery to an on-board computer (OBC).

The goal of I3DS is to demonstrate the processing on actual space HW, and therefore its ICU is based in a hybrid architecture containing different processing platforms that are compatible with space technologies.

The I3DS ICU is based in two different boards aiming to demonstrate the algorithms implementation in different architectures.

The first board is an FPGA SoC-based board containing an FPGA and an ARM-based microprocessor.

The second processing board is based on the LEON processor together with several Digital Processing Units that are implemented in an FPGA.

These two boards are interconnected via SpaceWire (SpW) links for controlling the 12 available sensors. As the selected set of sensors for I3DS are in the process of space qualification, their interfaces are not compatible with the ones usually used in a space environment and require an adaptation.

The first board contain a set of non-space interfaces (such as USB, Ethernet…), and is in charge of interfacing with most of the sensors. The second board is a board thought to be used for space developments and therefore interface with the sensors that have space-compatible interfaces being SpW, CAN, and SPI.

The companion FPGA present in the first board would implement the remaining sensor interfaces and will provide a SpW RMAP interface to the LEON in order to be able to command and control the FPGA sensor interfaces as well as pre-process some sensor data.

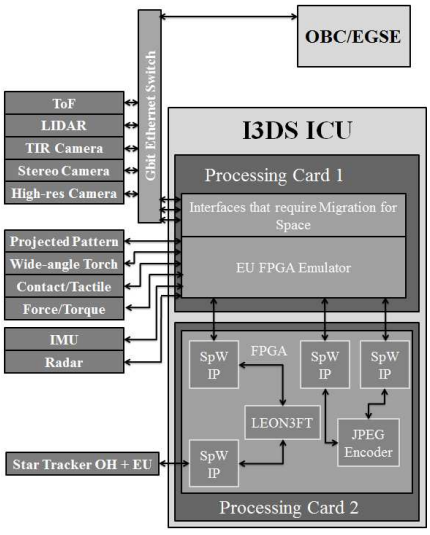

Figure 1: I3DS ICU architecture.

2.3 Processing parallelization

The architecture proposed in the Processing Board #2 is ideal for addressing both the controlling and processing needs of an ICU. The board is equipped with a LEON3FT [4] and Application Specific Processors (ASP) implemented in an FPGA working @ 100MHz. As the LEON3FT and the processing units have separate memory buses, they are able to operate independently of each other and therefore is possible to isolate different tasks.

Taking advantage of the task isolation the proposed architecture can be divided in two major subsystems, based on their main scope:

- **Control**, with a General-Purpose Processor (GPP) at its heart, providing general control tasks;
- **Processing**, with companion processors (ASPs) implemented in an FPGA providing the raw processing power together with high-speed I/O.

In that way the LEON processor will be in charge of the control of the different sensors and the communication with the FPGA and the final on-board computer while the ASPs will be processing the data acquired by the different sensors in a coordinated manner.

The Processing Card prototype is based on a GR-XCKU Development Board developed by Thales Alenia Space in the frame of the SSDP project and commercialized by Cobham Gaisler which comprises a custom designed PCB so that the board could work as a stand-alone bench top development. This board includes a Xilinx Kintex Ultrascale XCKU060 FPGA. The interface connectors on the front edge of the board include four SpaceWire (SpW) interface that will be used for our use case.

The FPGA architecture design mainly have two functionalities parallelized (Figure 2):

- LEON3FT Processor: it is in charge of sending and receiving commands from Star Tracker (STR) sensor and also it process its data.
- JPEG Encoder: it compresses images coming from Processing Card 1 and then it returns them.

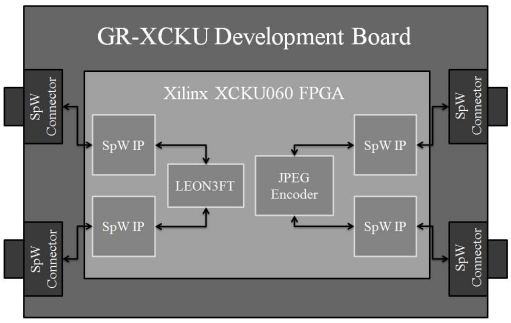

Figure 2: Processing Card 2 Architecture

In this architecture, measurements and status data are sent from the STR to the LEON3FT processor. Commands are sent and received in an alternated manner between sensor and processor. That is because they are treated differently.

In order to have two tasks running inside the processor at the same time, RTEMS (Real Time Executive for Multiprocessor Systems) will be executed by the LEON3FT processor (Figure 3).

The Main Task will compute command data. First it will receive commands from Processing Card. Then it will send them to STR Sensor. After that, it will receive STR command. Finally, the Main Task will send STR command to Processing Card #1.

Second Task will receive measurement and status from STR sensor. Then it will process them. Lastly, it will send processed data to Processing Card #1.

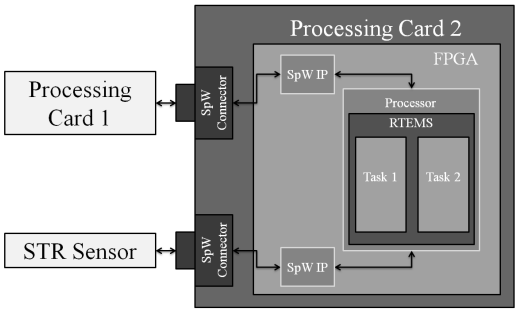

Figure 3: Command and control.

In order to demonstrate the parallelized architecture concept a JPEG encoder has been implemented in order to process and compress images received from the camera. It has been implemented on the FPGA in an isolated manner so the LEON processor does not interfere with its processing tasks. The JPEG encoder receives raw images through the SpaceWire communication interface with the following format:

- Number of layers: (i.e. 3 for RGB image)
- Number of rows: height of the image

- Number of columns: width of the image

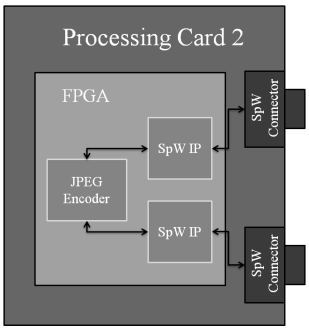

Figure 3: Image processing.

The JPEG encoder converts this input image in a compressed output image. Finally this compressed image is sent back through SpaceWire communication interface.

5 CONCLUSION

The huge amount of information generated by next-generation sensors is a challenge for the space processing platforms that are aimed to be used in robotics. The increasing processing power of new space qualified processors and the new generation of reconfigurable FPGAs promises to fill this gap but it is still necessary to cope with their limitations.

Space qualified HW (both microprocessors and FPGAs) do not have as many resources nor performance as the ones used for a ground environment. This is a huge limitation as it is necessary to adapt and optimize all the algorithms and developed frameworks to be included in an space qualified part and in last instance to dismiss some functionalities.

This paper has presented a survey of present possible Processor / FPGA based architectures, analysing their performance as well as their space environment compatibility. It also has introduced the needs of future architectures for the next generation processors / FPGAs.

This paper also presents the work that is being performed under the scope of the I3DS project where a possible use-case architecture has been selected. In this sense, the I3DS project has been always focused to make use of target architectures which are compatible with space, in order to implement the sensor processing algorithms and be able to demonstrate a real use-case. The goal of I3DS is to demonstrate the processing on actual Space HW, and therefore its ICU is based in a hybrid architecture containing different processing platforms that are compatible with space technologies. In this context a parallelization use case where processing and command and control are running together has been selected as a way to demonstrate this architecture feasibility.

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References

[1] Scalable Sensor Data Processor: Architecture and Development Status, R. Pinto, L. Berrojo, E. Garcia, R. Trautner, G. Rauwerda, K. Sunesen, S. Redant, S. Habinc, J. Andersson, J. López, ESA DSP Day, Gothenborg, 2016.

[2] DAHLIA Deep sub-micron microprocessor for spAce rad-Hard appLIcation Asic. Available: http:// dahlia-h2020.eu

[3] Xilinx Virtex-5QV Update and Space Roadmap. Kangsen Huey. 17th, March, 2016. SEFUW: SpacE FPGA Users Workshop, 3rd Edition.

[4] Xilinx On-Orbit Reconfigurable Kintex UltraScale FPGA Technology for Space. Daniel Elftmann. 9th April 2018.SEFUW: SpacE FPGA Users Workshop, 4rd Edition.

[5] GSTP-6 Element 1 Compendium of Potential Activities - ESA – emits. Available at: http://emits.sso.esa.int/emits-doc/ESTEC/News/GSTP6_E1-Compendium2016Rev2.pdf

[6] European Space Agency Science Programme Technology Development Plan: Programme of Work for 2017/2018 and Related Procurement Plan. Available at: http://sci.esa.int/sci-ft/47731-european-space-agency-science-programme-technology-development-plan-programme-of-work-for-2017-2018/#

[7] Generic AOCS/GNC techniques and design framework for Failure Detection Isolation and Recovery (G617-035EC).

[8] PERASPERA - "COMPET-4-2014: Space Robotic Technologies“ H2020 Work Programme 2014 topic (Grant Agreement (GA) number: 640026) [Online]. Available: http://www.h2020-peraspera.eu/

[9] I3DS – “Integrated 3D Sensor Suite” H2020 research and innovation programme. Grant Agreement no 730118) [Online]. Available: http://i3ds-h2020.eu/